multiplexing or no multiplexing at all and any form of modulation, and having a clock input coupled to said clock output of said master clock, and having a data input for receiving downstream data and having a data output at which symbols to be transmitted downstream appear;

a downstream mixer having a data input coupled to said data output of said downstream modulator and having a carrier input for receiving a downstream carrier, and having a data output for coupling to a transmission media;

B1 Cont.

an upstream clock generator having a clock input coupled to said clock output of said master clock and having an upstream clock output at which appears an upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal where M and N are integers;

a frequency divider having a clock input coupled to said upstream clock output of said upstream clock generator and having a carrier clock output at which a carrier clock signal appears;

a downstream carrier synthesizer coupled to receive said carrier clock signal from said frequency divider and having an output at which appears a downstream carrier signal which is phase coherent with said downstream clock signal and which is coupled to said carrier input of said downstream mixer;

an upstream carrier synthesizer having a clock input coupled to said carrier clock output of said frequency divider, and having an upstream carrier output at which appears an upstream carrier signal which is phase coherent with said master downstream clock signal;

an upstream mixer having a carrier input coupled to said upstream carrier output of said upstream carrier synthesizer, and having an input for

coupling to a transmission media to receive upstream signals, and having an output at which baseband demodulated upstream signals appear;

B1 Cont.

an upstream demodulator/demultiplexer implementing any form of TDMA or SCDMA or CDMA demultiplexing, or no demultiplexing at all if the incoming data is not multiplexed, and which implements any form of demodulation, and which is capable of carrying out prior art ranging or other processes to achieve frame synchronization or alignment of minislot boundaries of the transmitted signal to minislot boundaries in said data transceiver, and having a clock input coupled to said upstream clock output of said [master clock] upstream clock generator, said upstream demodulator/demultiplexer having an input coupled to receive said baseband demodulated upstream signals, and having an output at which appears recovered upstream data.

Remarks

The amendment to claim 3 corrects the connection of the clock input of the